**Chapter 2**

1. The \_\_\_\_\_\_\_\_\_ was the world’s first general-purpose electronic digital computer.

A. UNIVAC B. MARK IV

C. ENIAC D. Hollerith’s Counting Machine

2. The Electronic Numerical Integrator and Computer project was a response to U.S. needs during \_\_\_\_\_\_\_\_\_.

A. the Civil War B. the French-American War

C. World War I D. World War II

3. The ENIAC used \_\_\_\_\_\_\_\_\_\_.

A. vacuum tubes B. integrated circuits

C. IAS D. transistors

4. The ENIAC is an example of a \_\_\_\_\_\_\_\_\_ generation computer.

A. first B. second

C. third D. fourth

5. The \_\_\_\_\_\_\_\_\_\_ interprets the instructions in memory and causes them to be executed.

A. main memory B. control unit

C. I/O D. arithmetic and logic unit

6. The memory of the IAS consists of 1000 storage locations called \_\_\_\_\_\_\_\_\_\_.

A. opcodes B. wafers

C. VLSIs D. words

7. The \_\_\_\_\_\_\_\_\_\_ contains the 8-bit opcode instruction being executed.

A. memory buffer register B. instruction buffer register

C. instruction register D. memory address register

8. During the \_\_\_\_\_\_\_\_\_ the opcode of the next instruction is loaded into the IR and the address portion is loaded into the MAR.

A. execute cycle B. fetch cycle

C. instruction cycle D. clock cycle

9. Second generation computers used \_\_\_\_\_\_\_\_\_\_.

A. integrated circuits B. transistors

C. vacuum tubes D. large-scale integration

10. The \_\_\_\_\_\_\_\_\_\_ defines the third generation of computers.

A. integrated circuit B. vacuum tube

C. transistor D. VLSI

11. The use of multiple processors on the same chip is referred to as \_\_\_\_\_\_\_\_\_\_ and provides the potential to increase performance without increasing the clock rate.

A. multicore B. GPU

C. data channels D. MPC

12. With the \_\_\_\_\_\_\_\_\_\_, Intel introduced the use of superscalar techniques that allow multiple instructions to execute in parallel.

A. Core B. 8080

C. 80486 D. Pentium

13. The \_\_\_\_\_\_\_\_\_\_ measures the ability of a computer to complete a single task.

A. clock speed B. speed metric

C. execute cycle D. cycle time

14. ARM processors are designed to meet the needs of \_\_\_\_\_\_\_\_\_.

A. embedded real-time systems B. application platforms

C. secure applications D. all of the above

15. One increment, or pulse, of the system clock is referred to as a \_\_\_\_\_\_\_\_\_.

A. clock tick B. cycle time

C. clock rate D. cycle speed

**Chapter 3:**

1. Virtually all contemporary computer designs are based on concepts developed by \_\_\_\_\_\_\_\_\_\_ at the Institute for Advanced Studies, Princeton.  
   a. John Maulchy  
   b. John von Neumann  
   c. Herman Hollerith  
   d. John Eckert
2. A sequence of codes or instructions is called \_\_\_\_\_\_\_\_\_\_.  
   a. software  
   b. memory  
   c. an interconnect  
   d. a register
3. The processing required for a single instruction is called a(n) \_\_\_\_\_\_\_\_\_\_ cycle.  
   a. execute  
   b. fetch  
   c. instruction  
   d. packet
4. A(n) \_\_\_\_\_\_\_\_\_ is generated by a failure such as power failure or memory parity error.  
   a. I/O interrupt  
   b. hardware failure interrupt  
   c. timer interrupt  
   d. program interrupt
5. A(n) \_\_\_\_\_\_\_\_\_ is generated by some condition that occurs as a result of an instruction execution.  
   a. timer interrupt  
   b. I/O interrupt  
   c. program interrupt  
   d. hardware failure interrupt
6. A bus that connects major computer components (processor, memory, I/O) is called a \_\_\_\_\_\_\_\_\_\_.  
   a. system bus  
   b. address bus  
   c. data bus  
   d. control bus
7. The \_\_\_\_\_\_\_\_\_\_ are used to designate the source or destination of the data on the data bus.  
   a. system lines  
   b. data lines  
   c. control lines  
   d. address lines
8. The data lines provide a path for moving data among system modules and are collectively called the \_\_\_\_\_\_\_\_\_.  
   a. control bus  
   b. address bus  
   c. data bus  
   d. system bus
9. A \_\_\_\_\_\_\_\_\_\_ is the high-level set of rules for exchanging packets of data between devices.  
   a. bus  
   b. protocol  
   c. packet  
   d. QPI
10. Each data path consists of a pair of wires (referred to as a \_\_\_\_\_\_\_\_\_\_) that transmits data one bit at a time.  
    a. lane  
    b. path  
    c. line  
    d. bus
11. The \_\_\_\_\_\_\_\_\_ receives read and write requests from the software above the TL and creates request packets for transmission to a destination via the link layer.  
    a. transaction layer  
    b. root layer  
    c. configuration layer  
    d. transport layer
12. The TL supports which of the following address spaces?  
    a. memory  
    b. I/O  
    c. message  
    d. all of the above
13. The QPI \_\_\_\_\_\_\_\_\_ layer is used to determine the course that a packet will traverse across the available system interconnects.  
    a. link  
    b. protocol  
    c. routing  
    d. physical

**Chapter 4:**

1. \_\_\_\_\_\_\_\_\_\_ refers to whether memory is internal or external to the computer.  
   A. Location  
   B. Access  
   C. Hierarchy  
   D. Tag
2. Internal memory capacity is typically expressed in terms of \_\_\_\_\_\_\_\_\_.  
   A. Hertz  
   B. Nanos  
   C. Bytes  
   D. LOR
3. For internal memory, the \_\_\_\_\_\_\_\_\_\_ is equal to the number of electrical lines into and out of the memory module.  
   A. Access time  
   B. Unit of transfer  
   C. Capacity  
   D. Memory ratio
4. "Memory is organized into records and access must be made in a specific linear sequence" is a description of \_\_\_\_\_\_\_\_\_\_.  
   A. Sequential access  
   B. Direct access  
   C. Random access  
   D. Associative
5. individual blocks or records have a unique address based on physical location with \_\_\_\_\_\_\_\_\_\_.  
   A. Associative  
   B. Physical access  
   C. Direct access  
   D. Sequential access
6. For random-access memory, \_\_\_\_\_\_\_\_\_\_ is the time from the instant that an address is presented to the memory to the instant that data have been stored or made available for use.  
   A. Memory cycle time  
   B. Direct access  
   C. Transfer rate  
   D. Access time
7. The \_\_\_\_\_\_\_\_ consists of the access time plus any additional time required before a second access can commence.  
   A. Latency  
   B. Memory cycle time  
   C. Direct access  
   D. Transfer rate
8. A portion of main memory used as a buffer to hold data temporarily that is to be read out to disk is referred to as a \_\_\_\_\_\_\_\_\_.  
   A. Disk cache  
   B. Latency  
   C. Virtual address  
   D. Miss
9. A line includes a \_\_\_\_\_\_\_\_\_ that identifies which particular block is currently being stored.  
   A. Cache  
   B. Hit  
   C. Tag  
   D. Locality
10. \_\_\_\_\_\_\_\_\_\_ is the simplest mapping technique and maps each block of main memory into only one possible cache line.  
    A. Direct mapping  
    B. Associative mapping  
    C. Set associative mapping  
    D. None of the above
11. When using the \_\_\_\_\_\_\_\_\_\_ technique all write operations made to main memory are made to the cache as well.  
    A. Write back  
    B. LRU  
    C. Write through  
    D. Unified cache
12. The key advantage of the \_\_\_\_\_\_\_\_\_\_ design is that it eliminates contention for the cache between the instruction fetch/decode unit and the execution unit.  
    A. Logical cache  
    B. Split cache  
    C. Unified cache  
    D. Physical cache
13. The Pentium 4 \_\_\_\_\_\_\_\_\_ component executes micro-operations, fetching the required data from the L1 data cache and temporarily storing results in registers.  
    A. Fetch/decode unit  
    B. Out-of-order execution logic  
    C. Execution unit  
    D. Memory subsystem
14. In reference to access time to a two-level memory, a \_\_\_\_\_\_\_\_\_ occurs if an accessed word is not found in the faster memory.  
    A. Miss  
    B. Hit  
    C. Line  
    D. Tag
15. A logical cache stores data using \_\_\_\_\_\_\_\_\_\_.  
    A. Physical addresses  
    B. Virtual addresses  
    C. Random addresses  
    D. None of the above

**Chapter 5:**

1. Which properties do all semiconductor memory cells share?  
   a. they exhibit two stable states which can be used to represent binary 1 and 0  
   b. they are capable of being written into to set the state  
   c. they are capable of being read to sense the state  
   d. all of the above
2. One distinguishing characteristic of memory that is designated as \_\_\_\_\_\_\_\_\_ is that it is possible to both to read data from the memory and to write new data into the memory easily and rapidly.  
   a. RAM  
   b. ROM  
   c. EPROM  
   d. EEPROM
3. Which of the following memory types are nonvolatile?  
   a. erasable PROM  
   b. programmable ROM  
   c. flash memory  
   d. all of the above
4. In a \_\_\_\_\_\_\_\_\_, binary values are stored using traditional flip-flop logic-gate configurations.  
   a. ROM  
   b. SRAM  
   c. DRAM  
   d. RAM
5. A \_\_\_\_\_\_\_\_\_\_ contains a permanent pattern of data that cannot be changed, is nonvolatile, and cannot have new data written into it.  
   a. RAM  
   b. SRAM  
   c. ROM  
   d. flash memory
6. With \_\_\_\_\_\_\_\_\_ the microchip is organized so that a section of memory cells are erased in a single action.  
   a. flash memory  
   b. SDRAM  
   c. DRAM  
   d. EEPROM
7. \_\_\_\_\_\_\_\_\_\_ can be caused by harsh environmental abuse, manufacturing defects, and wear.  
   a. SEC errors  
   b. Hard errors  
   c. Syndrome errors  
   d. Soft errors
8. 8 \_\_\_\_\_\_\_\_\_ can be caused by power supply problems or alpha particles.  
   a. Soft errors  
   b. AGT errors  
   c. Hard errors  
   d. SEC errors
9. 9 The \_\_\_\_\_\_\_\_\_ exchanges data with the processor synchronized to an external clock signal and running at the full speed of the processor/memory bus without imposing wait states.  
   a. DDR-DRAM  
   b. SDRAM  
   c. CDRAM  
   d. none of the above
10. 10 \_\_\_\_\_\_\_\_ can send data to the processor twice per clock cycle.  
    a. CDRAM  
    b. SDRAM  
    c. DDR-DRAM  
    d. RDRAM
11. 11 \_\_\_\_\_\_\_\_\_\_ increases the data transfer rate by increasing the operational frequency of the RAM chip and by increasing the prefetch buffer from 2 bits to 4 bits per chip.  
    a. DDR2  
    b. RDRAM  
    c. CDRAM  
    d. DDR3
12. 12 \_\_\_\_\_\_\_\_ increases the prefetch buffer size to 8 bits.  
    a. CDRAM  
    b. RDRAM  
    c. DDR3  
    d. all of the above
13. 13 Theoretically, a DDR module can transfer data at a clock rate in the range of \_\_\_\_\_\_\_\_\_\_ MHz.  
    a. 200 to 600  
    b. 400 to 1066  
    c. 600 to 1400  
    d. 800 to 1600
14. 14 A DDR3 module transfers data at a clock rate of \_\_\_\_\_\_\_\_\_\_ MHz.  
    a. 600 to 1200  
    b. 800 to 1600  
    c. 1000 to 2000  
    d. 1500 to 3000
15. 5 The \_\_\_\_\_\_\_\_ enables the RAM chip to preposition bits to be placed on the data bus as rapidly as possible.  
    a. flash memory  
    b. Hamming code  
    c. RamBus  
    d. buffer

**Chapter 6: External Memorygt**

1. Greater ability to withstand shock and damage, improvement in the uniformity of the magnet film surface to increase disk reliability, and a significant reduction in overall surface defects to help reduce read-write errors, are all benefits of \_\_\_\_\_\_\_\_\_\_\_.

A. magnetic read and write mechanisms

B. platters

C. the glass substrate

D. a solid state drive

2. Adjacent tracks are separated by \_\_\_\_\_\_\_\_\_.

A. sectors B. gaps

C. pits D. heads

3. Data are transferred to and from the disk in \_\_\_\_\_\_\_\_\_\_.

A. tracks B. gaps

C. sectors D. pits

4. In most contemporary systems fixed-length sectors are used, with \_\_\_\_\_\_\_\_\_ bytes being the nearly universal sector size.

A. 64 B. 128

C. 256 D. 512

5. Scanning information at the same rate by rotating the disk at a fixed speed is known as the \_\_\_\_\_\_\_\_\_.

A. constant angular velocity B. magnetoresistive

C. rotational delay D. constant linear velocity

6. The disadvantage of \_\_\_\_\_\_\_\_\_ is that the amount of data that can be stored on the long outer tracks is only the same as what can be stored on the short inner tracks.

A. SSD B. CAV

C. ROM D. CLV

7. A \_\_\_\_\_\_\_\_\_\_ disk is permanently mounted in the disk drive, such as the hard disk in a personal computer.

A. nonremovable B. movable-head

C. double sided D. removable

8. When the magnetizable coating is applied to both sides of the platter the disk is then referred to as \_\_\_\_\_\_\_\_\_.

A. multiple sided B. substrate

C. double sided D. all of the above

9. The set of all the tracks in the same relative position on the platter is referred to as a \_\_\_\_\_\_\_\_\_.

A. floppy disk B. single-sided disk

C. sector D. cylinder

10. The sum of the seek time and the rotational delay equals the \_\_\_\_\_\_\_\_\_, which is the time it takes to get into position to read or write.

A. access time B. gap time

C. transfer time D. constant angular velocity

11. \_\_\_\_\_\_\_\_\_\_ is the standardized scheme for multiple-disk database design.

A. RAID B. CAV

C. CLV D. SSD

12. RAID level \_\_\_\_\_\_\_\_ has the highest disk overhead of all RAID types.

A. 0 B. 1

C. 3 D. 5

13. A \_\_\_\_\_\_\_\_\_ is a high-definition video disk that can store 25 Gbytes on a single layer on a single side.

A. DVD B. DVD-R

C. DVD-RW D. Blu-ray DVD

14. \_\_\_\_\_\_\_\_ is when the disk rotates more slowly for accesses near the outer edge than for those near the center.

A. Constant angular velocity (CAV) B. Magnetoresistive

C. Constant linear velocity (CLV) D. Seek time

15. The areas between pits are called \_\_\_\_\_\_\_\_\_.

A. lands B. sectors

C. cylinders D. strips

**Chapter 7: Input Output**

1. The \_\_\_\_\_\_\_\_\_ contains logic for performing a communication function between the peripheral and the bus.

A. I/O channel B. I/O module

C. I/O processor D. I/O command

2. The most common means of computer/user interaction is a \_\_\_\_\_\_\_\_\_\_.

A. keyboard/monitor B. mouse/printer

C. modem/printer D. monitor/printer

3. The I/O function includes a \_\_\_\_\_\_\_\_\_ requirement to coordinate the flow of traffic between internal resources and external devices.

A. cycle B. status reporting

C. control and timing D. data

4. An I/O module that takes on most of the detailed processing burden, presenting a high-level interface to the processor, is usually referred to as an \_\_\_\_\_\_\_\_\_.

A. I/O channel B. I/O command

C. I/O controller D. device controller

5. An I/O module that is quite primitive and requires detailed control is usually referred to as an \_\_\_\_\_\_\_\_\_.

A. I/O command B. I/O controller

C. I/O channel D. I/O processor

6. The \_\_\_\_\_\_\_\_\_ command causes the I/O module to take an item of data from the data bus and subsequently transmit that data item to the peripheral.

A. control B. test

C. read D. write

7. The \_\_\_\_\_\_\_\_ command is used to activate a peripheral and tell it what to do.

A. control B. test

C. read D. write

8. \_\_\_\_\_\_\_\_ is when the DMA module must force the processor to suspend operation temporarily.

A. Interrupt B. Thunderbolt

C. Cycle stealing D. Lock down

9. The 8237 DMA is known as a \_\_\_\_\_\_\_\_\_ DMA controller.

A. command B. cycle stealing

C. interrupt D. fly-by

10. \_\_\_\_\_\_\_\_ is a digital display interface standard now widely adopted for computer monitors, laptop displays, and other graphics and video interfaces.

C. Thunderbolt D. InfiniBand

A. DisplayPort B. PCI Express

11. The \_\_\_\_\_\_\_\_ layer is the key to the operation of Thunderbolt and what makes it attractive as a high-speed peripheral I/O technology.

A. cable B. application

C. common transport D. physical

12. The Thunderbolt protocol \_\_\_\_\_\_\_\_\_ layer is responsible for link maintenance including hot-plug detection and data encoding to provide highly efficient data transfer.

A. cable B. application

C. common transport D. physical

13. The \_\_\_\_\_\_\_\_ contains I/O protocols that are mapped on to the transport layer.

A. cable B. application

C. common transport D. physical

14. A \_\_\_\_\_\_\_\_ is used to connect storage systems, routers, and other peripheral devices to an InfiniBand switch.

A. target channel adapter B. InfiniBand switch

C. host channel adapter D. subnet

15. A \_\_\_\_\_\_\_\_ connects InfiniBand subnets, or connects an InfiniBand switch to a network such as a local area network, wide area network, or storage area network.

A. memory controller B. TCA

C. HCA D. router

**Chapter 8: Operating System Support**

1. The \_\_\_\_\_\_\_\_\_\_ is a program that controls the execution of application programs and acts as an interface between applications and the computer hardware.

A. job control language B. operating system

C. batch system D. nucleus

2. Facilities and services provided by the OS that assist the programmer in creating programs are in the form of \_\_\_\_\_\_\_\_\_ programs that are not actually part of the OS but are accessible through the OS.

A. utility B. multitasking

C. JCL (Job control language) D. logical address

3. The \_\_\_\_\_\_\_\_\_ defines the repertoire of machine language instructions that a computer can follow.

A. ABI B. API

C. HLL D. ISA

4. The \_\_\_\_\_\_\_\_\_ defines the system call interface to the operating system and the hardware resources and services available in a system through the user instruction set architecture.

A. HLL B. API

C. ABI D. ISA

5. The \_\_\_\_\_\_\_\_ gives a program access to the hardware resources and services available in a system through the user instruction set architecture supplemented with high-level language library calls.

A. JCL B. ISA

C. ABI D. API

6. A \_\_\_\_\_\_\_\_\_ system works only one program at a time.

A. batch B. uniprogramming

C. kernel D. privileged instruction

7. A \_\_\_\_\_\_\_\_\_ is a special type of programming language used to provide instructions to the monitor.

A. job control language B. multiprogram

C. kernel D. utility

8. The \_\_\_\_\_\_\_\_\_ scheduler determines which programs are admitted to the system for processing.

A. long-term B. medium-term

C. short-term D. I/O

9. The \_\_\_\_\_\_\_\_ scheduler is also known as the dispatcher.

A. long-term B. medium-term

C. short-term D. I/O

10. A \_\_\_\_\_\_\_\_\_ is an actual location in main memory.

A. logical address B. partition address

C. base address D. physical address

11. \_\_\_\_\_\_\_\_ is when the processor spends most of its time swapping pages rather than executing instructions.

A. Swapping B. Thrashing

C. Paging D. Multitasking

12. Virtual memory schemes make use of a special cache called a \_\_\_\_\_\_\_\_ for page table entries.

A. TLB B. HLL

C. VMC D. SPB

13. With \_\_\_\_\_\_\_\_\_ the virtual address is the same as the physical address.

A. unsegmented unpaged memory B. unsegmented paged memory

C. segmented unpaged memory D. segmented paged memory

14. A \_\_\_\_\_\_\_\_\_ is a collection of memory regions.

A. APX B. nucleus

C. domain D. page table

15. The OS maintains a \_\_\_\_\_\_\_\_\_\_ for each process that shows the frame location for each page of the process.

A. kernel B. page table

C. TLB D. logical address

**Chapter 9:**

1.A sequence of hexadecimal digits can be thought of as representing an integer in base 10.  
(T/F)

T

2.Because of the inherent binary nature of digital computer components, all forms of data within computers are represented by various binary codes.  
(T/F) T

3.The decimal system has a base of \_\_\_\_\_\_\_\_\_.  
A. 0  
B. 10  
C. 100  
D. 1000

4.Which digit represents "hundreds" in the number 8732?  
A. 8  
B. 7  
C. 3  
D. 2

5.Which of the following is correct?  
A. 25 = (2 x 10^2) + (5 x 10^1)  
B. 289 = (2 x 10^3) + (8 x 10^1) + (9 x 10^0)  
C. 7523 = (7 x 10^3) + (5 x 10^2) + (2 x 10^1) + (3 x 10^0)  
D. 0.628 = (6 x 10^-3) + (2 x 10^-2) + (8 x 10^-1)

6.In the number 3109, the 3 is referred to as the \_\_\_\_\_\_\_\_\_.  
A. most significant digit  
B. least significant digit  
C. radix  
D. base

7.In the number 3109, the 9 is referred to as the \_\_\_\_\_\_\_\_\_.  
A. most significant digit  
B. least significant digit  
C. radix  
D. base

8Numbers in the binary system are represented to the \_\_\_\_\_\_\_\_\_.  
A. base 0  
B. base 1  
C. base 2  
D. base 10

9.Hexadecimal has a base of \_\_\_\_\_\_\_\_\_.  
A. 2  
B. 8  
C. 10  
D. 16

10.The binary string 110111100001 is equivalent to \_\_\_\_\_\_\_\_\_\_.  
A. DE1 (16)  
B. C78 (16)  
C. FF64 (16)  
D. B8F (16)

11.The \_\_\_\_\_\_\_\_\_ system uses only the numbers 0 and 1.  
A. positional  
B. binary  
C. hexadecimal  
D. decimal

12.Decimal "10" is \_\_\_\_\_\_\_\_\_\_ in binary.  
A. 1000  
B. 0010  
C. 1010  
D. 0001

13.Decimal "10" is \_\_\_\_\_\_\_\_\_ in hexadecimal.  
A. 1  
B. A  
C. 0  
D. FF

14.Four bits is called a \_\_\_\_\_\_\_\_\_.  
A. radix point  
B. byte  
C. nibble  
D. binary digit

15.Another term for "base" is \_\_\_\_\_\_\_\_\_\_.  
A. radix  
B. integer  
C. position  
D. digit

16.In the number 472.156 the 2 is the \_\_\_\_\_\_\_\_\_.  
A. most significant digit  
B. radix point  
C. least significant digit  
D. none of the above

17.Binary 0101 is hexadecimal \_\_\_\_\_\_\_\_\_.  
A. 0  
B. 5  
C. A  
D. 10

T

**Chapter 11: Digital Logic**

1. The operand \_\_\_\_\_\_\_\_ yields true if and only if both of its operands are true.

A. XOR B. OR

C. AND D. NOT

2. The operation \_\_\_\_\_\_\_\_\_ yields true if either or both of its+ operands are true.

A. NOT B. AND

C. NAND D. OR

3. The unary operation \_\_\_\_\_\_\_\_\_ inverts the value of its operand.

A. OR B. NOT

C. NAND D. XOR

4. A \_\_\_\_\_\_\_ is an electronic circuit that produces an output signal that is a simple Boolean operation on its input signals.

A. gate B. decoder

C. counter D. flip-flop

5. Which of the following is a functionally complete set?

A. AND, NOT B. NOR

C. AND, OR, NOT D. all of the above

6. For more than four variables an alternative approach is a tabular technique referred to as the \_\_\_\_\_\_\_\_\_ method.

A. DeMorgan B. Quine-McCluskey

C. Karnaugh map D. Boole-Shannon

7. \_\_\_\_\_\_\_\_ are used in digital circuits to control signal and data routing.

A. Multiplexers B. Program counters

C. Flip-flops D. Gates

8. \_\_\_\_\_\_\_\_ is implemented with combinational circuits.

A. Nano memory B. Random access memory

C. Read only memory D. No memory

9. The \_\_\_\_\_\_\_\_ exists in one of two states and, in the absence of input, remains in that state.

A. assert B. complex PLD

C. decoder **D. flip-flop**

10. The \_\_\_\_\_\_\_\_ flip-flop has two inputs and all possible combinations of input values are valid.

A. J-K B. D

C. S-R D. clocked S-R

11. A \_\_\_\_\_\_\_\_\_ accepts and/or transfers information serially.

A. S-R latch B. shift register

C. FPGA D. parallel register

12. Counters can be designated as \_\_\_\_\_\_\_\_\_.

A. asynchronous

B. synchronous

C. both asynchronous and synchronous

D. neither asynchronous or synchronous

13. CPUs make use of \_\_\_\_\_\_\_\_\_ counters, in which all of the flip-flops of the counter change at the same time.

A. synchronous B. asynchronous

C. clocked S-R D. timed ripple

14. The \_\_\_\_\_\_\_\_\_ table provides the value of the next output when the inputs and the present output are known, which is exactly the information needed to design the counter or any sequential circuit.

A. excitation B. Kenough

C. J-K flip-flop D. FPGA

15. A \_\_\_\_\_\_\_\_\_ is a PLD featuring a general structure that allows very high logic capacity and offers more narrow logic resources and a higher ration of flip-flops to logic resources than do CPLDs.

A. SPLD B. FPGA

C. PAL D. PLA

Chapter 12:

1. The \_\_\_\_\_\_\_\_ specifies the operation to be performed.

A. source operand reference B. opcode

C. next instruction reference D. processor register

1. A(n) \_\_\_\_\_\_\_\_\_ expresses operations in a concise algebraic form using variables.

A. opcode B. high-level language

C. machine language D. register

1. There must be \_\_\_\_\_\_\_\_ instructions for moving data between memory and the registers.

A. branch B. logic

C. memory D. I/O

1. \_\_\_\_\_\_\_\_ instructions operate on the bits of a word as bits rather than as numbers, providing capabilities for processing any other type of data the user may wish to employ.

A. Logic B. Arithmetic

C. Memory D. Test

1. \_\_\_\_\_\_\_\_\_ instructions provide computational capabilities for processing number data.

A. Boolean B. Logic

C. Memory D. Arithmetic

1. \_\_\_\_\_\_\_ instructions are needed to transfer programs and data into memory and the results of computations back out to the user.

A. I/O B. Transfer

C. Control D. Branch

1. The x86 data type that is a signed binary value contained in a byte, word, or doubleword, using twos complement representation is \_\_\_\_\_\_\_\_\_.

A. general B. ordinal

C. integer D. packed BCD

1. The most fundamental type of machine instruction is the \_\_\_\_\_\_\_\_\_ instruction.

A. conversion **B. data transfer**

C. arithmetic D. logical

1. The \_\_\_\_\_\_\_\_\_ instruction includes an implied address.

A. skip B. rotate

C. stack D. push

1. Which of the following is a true statement?
2. a procedure can be called from more than one location
3. a procedure call can appear in a procedure
4. each procedure call is matched by a return in the called program
5. all of the above
6. The entire set of parameters, including return address, which is stored for a procedure invocation is referred to as a \_\_\_\_\_\_\_\_\_.

A. branch B. stack frame

C. pop D. push

1. Which ARM operation category includes logical instructions (AND, OR, XOR), add and subtract instructions, and test and compare instructions?

A. data-processing instructions B. branch instructions

C. load and store instructions D. extend instructions

1. In the ARM architecture only \_\_\_\_\_\_\_\_\_ instructions access memory locations.

A. data processing B. status register access

C. load and store D. branch

1. Which data type is defined in MMX?

A. packed byte B. packed word

C. packed doubleword D. all of the above

1. A branch instruction in which the branch is always taken is \_\_\_\_\_\_\_\_\_.

A. conditional branch B. unconditional branch

C. jump D. bi-endian

Chapter 13

1. The advantage of \_\_\_\_\_\_\_\_\_\_ is that no memory reference other than the instruction fetch is required to obtain the operand.

A. direct addressing B. immediate addressing

C. register addressing D. stack addressing

1. The principal advantage of \_\_\_\_\_\_\_\_\_\_\_ addressing is that it is a very simple form of addressing.

A. displacement B. register

C. stack D. direct

1. \_\_\_\_\_\_\_\_\_\_ has the advantage of large address space, however it has the disadvantage of multiple memory references.

A. Indirect addressing B. Direct addressing

C. Immediate addressing D. Stack addressing

1. The advantages of \_\_\_\_\_\_\_\_\_ addressing are that only a small address field is needed in the instruction and no time-consuming memory references are required.

A. direct B. indirect

C. register D. displacement

1. \_\_\_\_\_\_\_\_\_\_ has the advantage of flexibility, but the disadvantage of complexity.

A. Stack addressing B. Displacement addressing

C. Direct addressing D. Register addressing

1. For \_\_\_\_\_\_\_\_\_, the address field references a main memory address and the referenced register contains a positive displacement from that address.

A. indexing B. base-register addressing

C. relative addressing D. all of the above

1. Indexing performed after the indirection is \_\_\_\_\_\_\_\_\_\_.

A. relative addressing B. autoindexing

C. postindexing D. preindexing

1. For the \_\_\_\_\_\_\_\_\_ mode, the operand is included in the instruction.

A. immediate B. base

C. register D. displacement

1. The only form of addressing for branch instructions is \_\_\_\_\_\_\_\_\_ addressing.

A. register B. relative

C. base D. immediate

1. Which of the following interrelated factors go into determining the use of the addressing bits?

A. number of operands B. number of register sets

C. address range D. all of the above

1. \_\_\_\_\_\_\_\_\_ is a principle by which two variables are independent of each other.

A. Opcode B. Orthogonality

C. Completeness D. Autoindexing

1. The \_\_\_\_\_\_\_\_\_ was designed to provide a powerful and flexible instruction set within the constraints of a 16-bit minicomputer.

A. PDP-1 B. PDP-8

C. PDP-11 D. PDP-10

1. The \_\_\_\_\_\_\_\_\_\_ byte consists of three fields: the Scale field, the Index field and the Base field.

A. SIB B. VAX

C. PDP-11 D. ModR/M

1. All instructions in the ARM architecture are \_\_\_\_\_\_\_\_\_\_ bits long and follow a regular format.

A. 8 B. 16

C. 32 D. 64

1. \_\_\_\_\_\_\_\_\_\_ is a design principle employed in designing the PDP-10 instruction set.

A. Orthogonality B. Completeness

C. Direct addressing D. All of the above

Chater 14

1. \_\_\_\_\_\_\_\_\_\_ are a set of storage locations.

A. Processors B. PSWs

C. Registers D. Control units

1. The \_\_\_\_\_\_\_\_ controls the movement of data and instructions into and out of the processor.

A. control unit B. ALU

C. shifter D. branch

1. \_\_\_\_\_\_\_\_ registers may be used only to hold data and cannot be employed in the calculation of an operand address.

A. General purpose B. Data

C. Address D. Condition code

1. \_\_\_\_\_\_\_\_\_\_ are bits set by the processor hardware as the result of operations.

A. MIPS B. Condition codes

C. Stacks D. PSWs

1. The \_\_\_\_\_\_\_\_\_ contains the address of an instruction to be fetched.

A. instruction register B. memory address register

C. memory buffer register D. program counter

1. The \_\_\_\_\_\_\_\_\_ contains a word of data to be written to memory or the word most recently read.

A. MAR B. PC

C. MBR D. IR

1. The \_\_\_\_\_\_\_\_ determines the opcode and the operand specifiers.

A. decode instruction B. fetch operands

C. calculate operands D. execute instruction

1. \_\_\_\_\_\_\_\_\_ is a pipeline hazard.

A. Control B. Resource

C. Data D. All of the above

1. A \_\_\_\_\_\_\_\_ hazard occurs when there is a conflict in the access of an operand location.

A. resource B. data

C. structural D. control

1. A \_\_\_\_\_\_\_\_\_ is a small, very-high-speed memory maintained by the instruction fetch stage of the pipeline and containing the *n* most recently fetched instructions in sequence.

A. loop buffer B. delayed branch

C. multiple stream D. branch prediction

1. The \_\_\_\_\_\_\_\_\_ is a small cache memory associated with the instruction fetch stage of the pipeline.

A. dynamic branch B. loop table

C. branch history table D. flag

1. The \_\_\_\_\_\_\_\_\_ stage includes ALU operations, cache access, and register update.

A. decode B. execute

C. fetch D. write back

1. \_\_\_\_\_\_\_\_ is used for debugging.

A. Direction flag B. Alignment check

C. Trap flag D. Identification flag

1. The ARM architecture supports \_\_\_\_\_\_\_ execution modes.

A. 2 B. 8

C. 11 D. 7

1. The OS usually runs in \_\_\_\_\_\_\_\_.

A. supervisor mode B. abort mode

C. undefined mode D. fast interrupt mode

Chapter 15

1. \_\_\_\_\_\_\_\_\_ determines the control and pipeline organization.

A. Calculation B. Execution sequencing

C. Operations performed D. Operands used

1. The Patterson study examined the dynamic behavior of \_\_\_\_\_\_\_\_\_ programs, independent of the underlying architecture.

A. HLL B. RISC

C. CISC D. all of the above

1. \_\_\_\_\_\_\_\_\_ is the fastest available storage device.

A. Main memory B. Cache

C. Register storage D. HLL

1. The first commercial RISC product was \_\_\_\_\_\_\_\_\_.

A. SPARC B. CISC

C. VAX D. the Pyramid

1. \_\_\_\_\_\_\_\_\_ instructions are used to position quantities in registers temporarily for computational operations.

A. Load-and-store B. Window

C. Complex D. Branch

1. Which stage is required for load and store operations?

A. I B. E

C. D D. all of the above

1. A \_\_\_\_\_\_\_\_ instruction can be used to account for data and branch delays.

A. SUB B. NOOP

C. JUMP D. all of the above

1. The instruction location immediately following the delayed branch is referred to as the \_\_\_\_\_\_\_\_.

A. delay load B. delay file

C. delay slot D. delay register

1. A tactic similar to the delayed branch is the \_\_\_\_\_\_\_\_\_, which can be used on LOAD instructions.

A. delayed load B. delayed program

C. delayed slot D. delayed register

1. The MIPS R4000 uses \_\_\_\_\_\_\_\_ bits for all internal and external data paths and for addresses, registers, and the ALU.

A. 16 B. 32

C. 64 D. 128

1. All MIPS R series processor instructions are encoded in a single \_\_\_\_\_\_\_\_ word format.

A. 4-bit B. 8-bit

C. 16-bit D. 32-bit

1. A \_\_\_\_\_\_\_\_\_ architecture is one that makes use of more, and more fine-grained pipeline stages.

A. parallel B. superpipelined

C. superscalar D. hybrid

1. The R4000 can have as many as \_\_\_\_\_\_\_ instructions in the pipeline at the same time.

A. 8 B. 10

C. 5 D. 3

1. SPARC refers to an architecture defined by \_\_\_\_\_\_\_\_.

A. Microsoft B. Apple

C. Sun Microsystems D. IBM

1. The R4000 pipeline stage where the instruction result is written back to the register file is the \_\_\_\_\_\_\_\_\_\_ stage.

A. write back B. tag check

C. data cache D. instruction execute

Chapter 16

1. The superscalar approach can be used on \_\_\_\_\_\_\_\_\_\_ architecture.

A. RISC B. CISC

C. neither RISC nor CISC D. both RISC and CISC

1. The essence of the \_\_\_\_\_\_\_\_ approach is the ability to execute instructions independently and concurrently in different pipelines.

A. scalar B. branch

C. superscalar D. flow dependency

1. Which of the following is a fundamental limitation to parallelism with which the system must cope?

A. procedural dependency B. resource conflicts

C. antidependency D. all of the above

1. The situation where the second instruction needs data produced by the first instruction to execute is referred to as \_\_\_\_\_\_\_\_\_\_.

A. true data dependency B. output dependency

C. procedural dependency D. antidependency

1. The instructions following a branch have a \_\_\_\_\_\_\_\_\_ on the branch and cannot be executed until the branch is executed.

A. resource dependency B. procedural dependency

C. output dependency D. true data dependency

1. \_\_\_\_\_\_\_\_ refers to the process of initiating instruction execution in the processor’s functional units.

A. Instruction issue B. In-order issue

C. Out-of-order issue D. Procedural issue

1. Instead of the first instruction producing a value that the second instruction uses, with \_\_\_\_\_\_\_\_\_\_\_ the second instruction destroys a value that the first instruction uses.

A. in-order issue B. resource conflict

C. antidependency D. out-of-order completion

1. \_\_\_\_\_\_\_\_ indicates whether this micro-op is scheduled for execution, has been dispatched for execution, or has completed execution and is ready for retirement.

A. State B. Memory address

C. Micro-op D. Alias register

1. \_\_\_\_\_\_\_\_\_\_ exists when instructions in a sequence are independent and thus can be executed in parallel by overlapping.

A. Flow dependency B. Instruction-level parallelism

C. Machine parallelism D. Instruction issue

1. \_\_\_\_\_\_\_\_\_ is determined by the number of instructions that can be fetched and executed at the same time and by the speed and sophistication of the mechanisms that the processor uses to find independent instructions.

A. Machine parallelism B. Instruction-level parallelism

C. Output dependency D. Procedural dependency

1. \_\_\_\_\_\_\_\_ is a protocol used to issue instructions.

A. Micro-ops B. Scalar

C. SIMD D. Instruction issue policy

1. \_\_\_\_\_\_\_\_ is used in scalar RISC processors to improve the performance of instructions that require multiple cycles.

A. In-order completion B. In-order issue

C. Out-of-order completion D. Out-of-order issue

1. Which of the following is a hardware technique that can be used in a superscalar processor to enhance performance?

A. duplication of resources B. out-of-order issue

C. renaming D. all of the above

1. The \_\_\_\_\_\_\_\_ introduced a full-blown superscalar design with out-of-order execution.

A. Pentium B. Pentium Pro

C. 386 D. 486

1. Utilizing a branch target buffer (BTB), the \_\_\_\_\_\_\_\_\_ uses a dynamic branch prediction strategy based on the history of recent executions of branch instructions.

A. 486 B. Pentium

C. Pentium 4 D. Pentium Pro

Chapter 17

1. A taxonomy first introduced by \_\_\_\_\_\_\_ is still the most common way of categorizing systems with parallel processing capability.

A. Randolph B. Flynn

C. von Neuman D. Desai

1. Uniprocessors fall into the \_\_\_\_\_\_\_ category of computer systems.

A. MIMD B. SIMD

C. SISD D. MISD

1. Vector and array processors fall into the \_\_\_\_\_\_\_\_ category of computer systems.

A. SIMD B. SISD

C. MISD D. MIMD

1. SMPs, clusters, and NUMA systems fit into the \_\_\_\_\_\_\_\_ category of computer systems.

A. SISD B. MIMD

C. SIMD D. MISD

1. A \_\_\_\_\_\_\_\_\_ problem arises when multiple copies of the same data can exist in different caches simultaneously, and if processors are allowed to update their own copies freely, an inconsistent view of memory can result.

A. cache coherence B. cluster

C. failover D. failback

1. Hardware-based solutions are generally referred to as cache coherence \_\_\_\_\_\_\_.

A. clusters B. streams

C. protocols D. vectors

1. A \_\_\_\_\_\_\_\_\_\_ is an instance of a program running on a computer.

A. process B. process switch

C. thread D. thread switch

1. A \_\_\_\_\_\_\_\_ is a dispatchable unit of work within a process that includes a processor context and its own data area for a stack.

A. process B. process switch

C. thread D. thread switch

1. Replicating the entire processor on a single chip with each processor handling separate threads is \_\_\_\_\_\_\_\_\_.

A. interleaved multithreading B. blocked multithreading

C. simultaneous multithreading D. chip multiprocessing

1. With no multithreading, \_\_\_\_\_\_\_\_\_ is the simple pipeline found in traditional RISC and CISC machines.

A. superscalar

B. single-threaded scalar

C. blocked multithreaded scalar

D. interleaved multithreaded scalar

11. \_\_\_\_\_\_\_\_\_ causes results issuing from one functional unit to be fed immediately into another functional unit and so on.

A. Chaining B. Rollover

C. Passive standby D. Pipelining

12. The \_\_\_\_\_\_\_\_ contains control fields, such as the vector count, that determine how many elements in the vector registers are to be processed.

A. vector-mask register B. vector-activity count

C. vector-status register D. vector-instruction register

13. Which of the following is an approach to vector computation?

A. pipelined ALU B. parallel ALU’s

C. parallel processors D. all of the above

14. An operation that switches the processor from one process to another by saving all the process control data, register, and other information for the first and replacing them with the process information for the second is:

A. resource ownership switch B. process switch

C. thread switch D. cluster switch

15. With \_\_\_\_\_\_\_\_ instructions are simultaneously issued from multiple threads to the execution units of a superscalar processor.

A. SMT B. single-threaded scalar

C. coarse-grained multithreading D. chip multiprocessing

Chapter 18

1. With \_\_\_\_\_\_\_, register banks are replicated so that multiple threads can share the use of pipeline resources.

A. SMT B. pipelining

C. scalar D. superscalar

1. \_\_\_\_\_\_\_\_\_ is where individual instructions are executed through a pipeline of stages so that while one instruction is executing in one stage of the pipeline, another instruction is executing in another stage of the pipeline.

A. Superscalar B. Scalar

C. Pipelining D. Simultaneous multithreading

1. \_\_\_\_\_\_\_\_\_ is when multiple pipelines are constructed by replicating execution resources, enabling parallel execution of instructions in parallel pipelines so long as hazards are avoided.

A. Vectoring B. Superscalar

C. Hybrid multithreading D. Pipelining

1. One way to control power density is to use more of the chip area for \_\_\_\_\_\_\_\_.

A. multicore B. cache memory

C. silicon D. resistors

1. Lotus Domino or Siebel CRM are examples of \_\_\_\_\_\_\_\_\_\_\_ applications.

A. threaded B. multi-process

C. Java D. multi-instance

1. Oracle database, SAP, and PeopleSoft are examples of \_\_\_\_\_\_\_\_ applications.

A. Java B. multithreaded native

C. multi-instance D. multi-process

1. \_\_\_\_\_\_\_ applications that can benefit directly from multicore resources include application servers such as Sun’s Java Application Server, BEA’s Weblogic, IBM’s Websphere, and the open-source Tomcat application server.

A. Multi-instance B. Multi-process

C. Java D. Threaded

1. Putting rendering on one processor, AI on another, and physics on another is an example of \_\_\_\_\_\_\_\_\_ threading.

A. coarse B. multi-instance

C. fine-grained D. hybrid

1. A loop that iterates over an array of data can be split up into a number of smaller parallel loops in individual threads that can be scheduled in parallel when using \_\_\_\_\_\_\_\_ threading.

A. multi-process B. fine-grained

C. hybrid D. coarse

1. The \_\_\_\_\_\_\_\_\_ is an example of splitting off a separate, shared L3 cache, with dedicated L1 and L2 caches for each core processor.

A. IBM 370 B. ARM11 MPCore

C. AMD Opteron D. Intel Core i7

1. The \_\_\_\_\_\_\_\_ connects to the external bus, known as the Front Side Bus, which connects to main memory, I/O controllers, and other processor chips.

A. L2 B. APIC

C. bus interface D. all of the above

1. The Intel Core i7-990X, introduced in 2008, implements \_\_\_\_\_\_ x86 SMT processors, each with a dedicated L2 cache, and with a shared L3 cache.

A. 2 B. 4

C. 6 D. 8

1. Processors are called \_\_\_\_\_\_\_\_.

A. dies B. cores

C. QPI D. interconnects

1. The \_\_\_\_\_\_\_\_ feature enables moving dirty data from one CPU to another without writing to L2 and reading the data back in from external memory.

A. migratory lines B. DDI

C. VFP unit D. IPIs

1. The \_\_\_\_\_\_\_\_ is responsible for maintaining coherency among L1 data caches.

A. VFP unit B. distributed interrupt controller

C. snoop control unit (SCU) D. watchdog